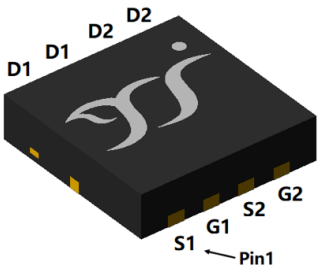
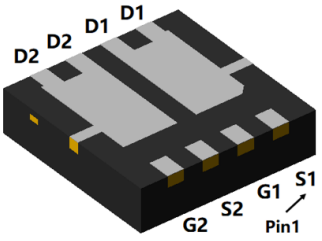
N-Channel and P-Channel Complementary MOSFET

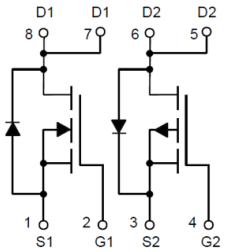


Top View



Bottom View

DFN3333-8L



Product Summary

NMOS

- V_{DS} 100V
- I_D 10A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜115mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜125mΩ
- 100% EAS Tested

PMOS

- V_{DS} -100V
- I_D -5.5A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜325mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜350mΩ
- 100% EAS Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC FAN
- Switching
- Motor drives

■ Absolute Maximum Ratings

Parameter	Conditions			Symbol	NMOS	PMOS	Unit
Drain-source Voltage				V_{DS}	100	-100	V
Gate-source Voltage				V_{GS}	±20	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃	NMOS: V_{GS}=10V	I_D	2.4	-1.5	A
			PMOS: V_{GS}=-10V				
		T_A=100℃	NMOS: V_{GS}=10V		1.5	-0.9	
			PMOS: V_{GS}=-10V				
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃	NMOS: V_{GS}=10V, Chip limitation		10	-5.5	
			PMOS: V_{GS}=-10V, Chip limitation				
		T_C =100℃	NMOS: V_{GS}=10V		6.3	-3.4	
			PMOS: V_{GS}=-10V				
Pulsed Drain Current	T_C=25℃, t_p=100μs			I_{DM}	30	-18	
Maximum Body-Diode Continuous Current	T_C=25℃			I_S	10	-5.5	
Avalanche energy	NMOS: T_J=25℃, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=8A			EAS	8	6.1	mJ
	PMOS: T_J=25℃, V_G=-10V, R_G=25Ω, L=0.5mH, I_{AS}=-7A						
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃		P_D	1.66	1.66	W
		T_A=100℃			0.66	0.66	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃			31	24	
		T_C =100℃			12.5	9.6	
Junction and Storage Temperature Range				T_J ,T_{STG}	-55～+150	-55～+150	℃

■Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	75	-	75	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	4	-	5.2	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ115NP10AJ	F1	115NP10A	5000	10000	100000	13'' reel

■ NMOS Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA, Tj=25℃	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V, Tj=25℃	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V, Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA, Tj=25℃	1.3	1.8	2.3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A, Tj=25℃	-	87	115	mΩ
		V_{GS}=4.5V, I_D=5A, Tj=25℃	-	88	125	
Diode Forward Voltage	V_{SD}	I_S=10A, V_{GS}=0V, Tj=25℃	-	0.9	1.2	V
Gate resistance	R_G	f=1MHz, Tj=25℃	-	1.7	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz, Tj=25℃	-	851	-	pF
Output Capacitance	C_{oss}		-	30	-	
Reverse Transfer Capacitance	C_{rss}		-	28	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=10A, Tj=25℃	-	23	-	nC
Gate-Source Charge	Q_{gs}		-	2.8	-	
Gate-Drain Charge	Q_{gd}		-	6.7	-	
Reverse Recovery Charge	Q_{rr}	I_F=10A, di/dt=100A/us, V_{GS}=0V, V_R=50V, Tj=25℃	-	37	-	nC
Reverse Recovery Time	t_{rr}		-	32	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DS}=50V, I_D=10A, R_L=5Ω, R_{GEN}=2.2Ω, Tj=25℃	-	8.5	-	ns
Turn-on Rise Time	t_r		-	20	-	
Turn-off Delay Time	$t_{D(off)}$		-	21	-	
Turn-off fall Time	t_f		-	2.2	-	

■ PMOS Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA, Tj=25℃	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V, Tj=25℃	-	-	-1	μA
		V_{DS}=-100V, V_{GS}=0V, Tj=150℃	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V, Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA, Tj=25℃	-1	-1.5	-2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-5A, Tj=25℃	-	250	325	mΩ
		V_{GS}=-4.5V, I_D=-3A, Tj=25℃	-	260	350	
Diode Forward Voltage	V_{SD}	I_S=-5A, V_{GS}=0V, Tj=25℃	-	-	-1.2	V
Gate resistance	R_G	f=1MHz, Tj=25℃	-	5	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-50V, V_{GS}=0V, f=1MHz, Tj=25℃	-	949	-	pF
Output Capacitance	C_{oss}		-	24	-	
Reverse Transfer Capacitance	C_{rss}		-	21	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-50V, I_D=-5A, Tj=25℃	-	18.4	-	nC
Gate-Source Charge	Q_{gs}		-	1.4	-	
Gate-Drain Charge	Q_{gd}		-	2.2	-	
Reverse Recovery Charge	Q_{rr}	I_F=-5A, di/dt=100A/us V_{GS}=0V, V_R=-50V, Tj=25℃	-	48.7	-	nC
Reverse Recovery Time	t_{rr}		-	28.4	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-50V, ID=-5A, R_L=10Ω, R_{GEN}=2.7Ω, Tj=25℃	-	7	-	ns
Turn-on Rise Time	t_r		-	32.4	-	
Turn-off Delay Time	$t_{D(off)}$		-	26.2	-	
Turn-off fall Time	t_f		-	6.4	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

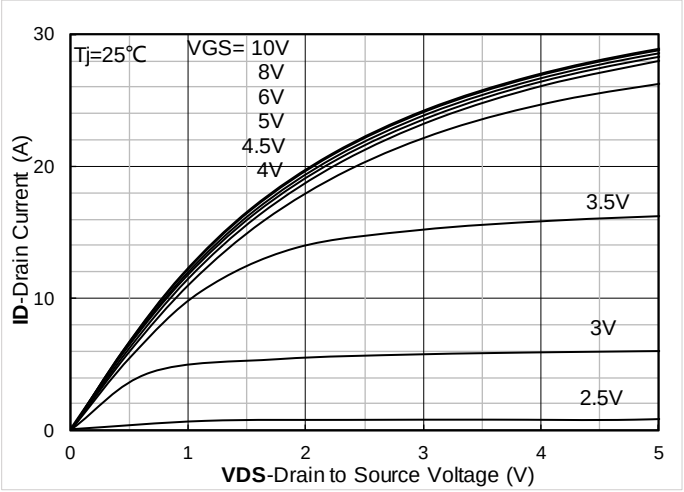


Figure 1. Output Characteristics; typical values

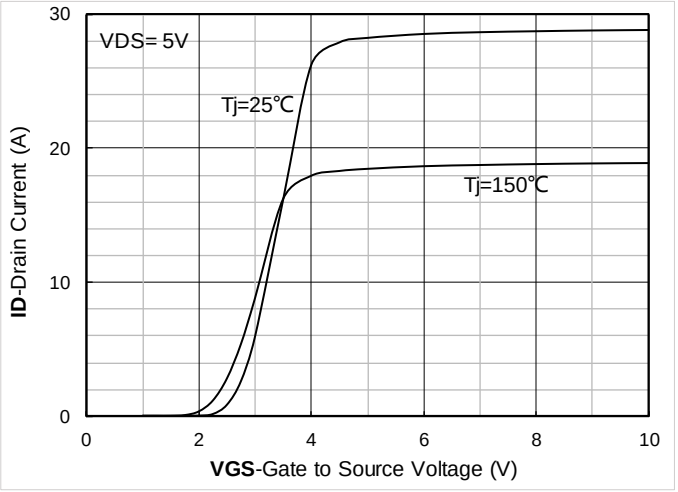


Figure 2. Transfer Characteristics; typical values

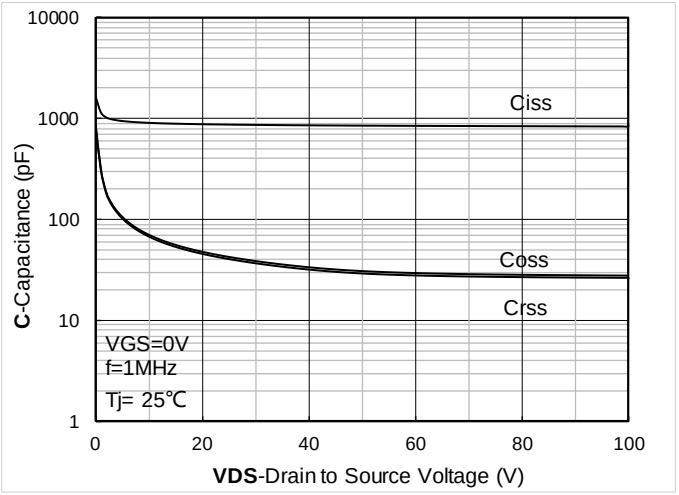


Figure 3. Capacitance Characteristics; typical values

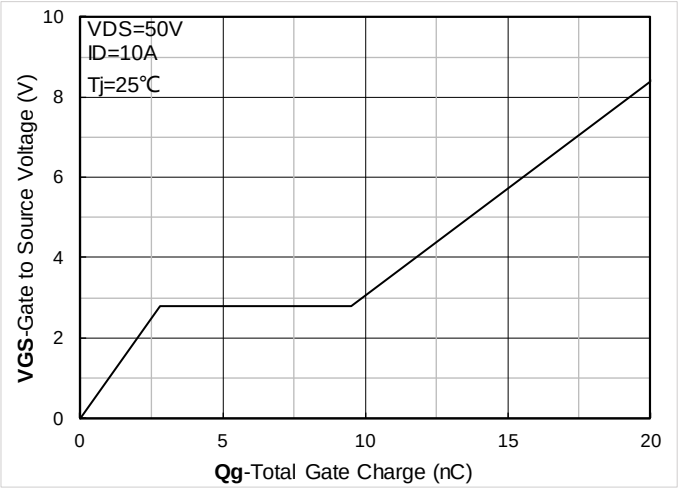


Figure 4. Gate Charge; typical values

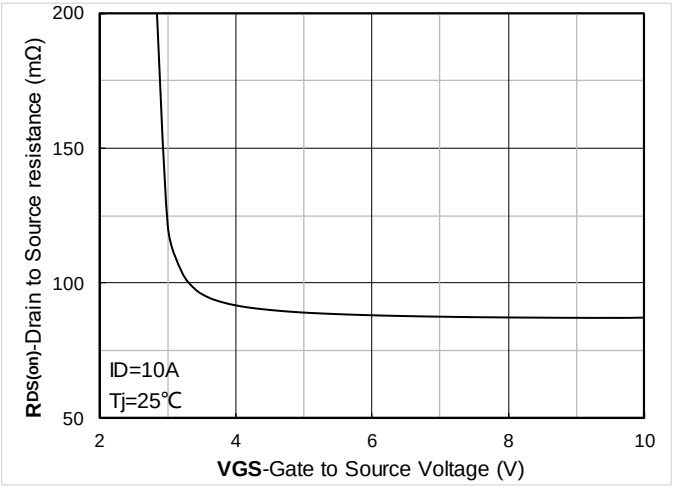


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

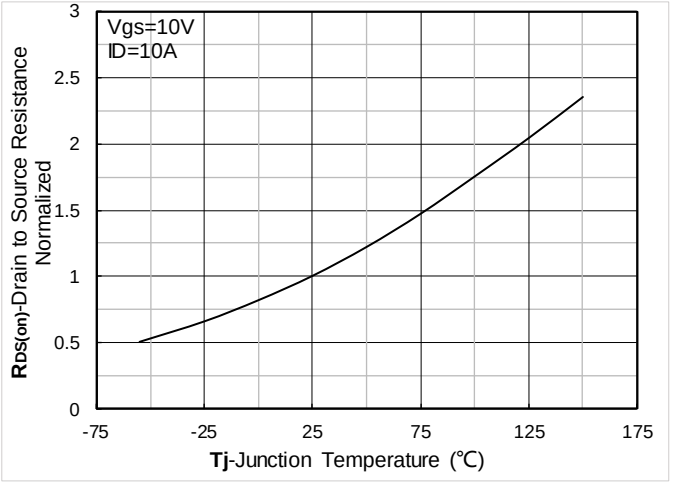


Figure 6. Normalized On-Resistance

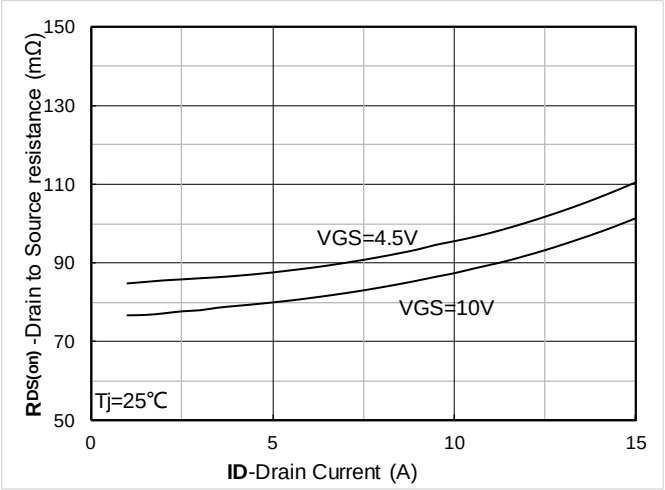


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

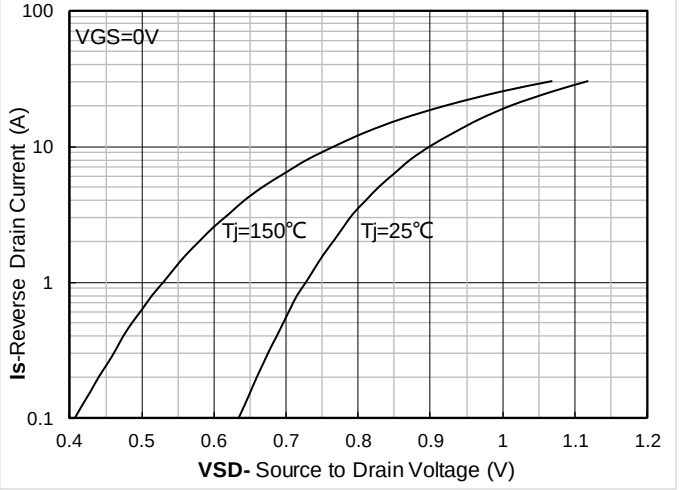


Figure 8. Forward characteristics of reverse diode; typical values

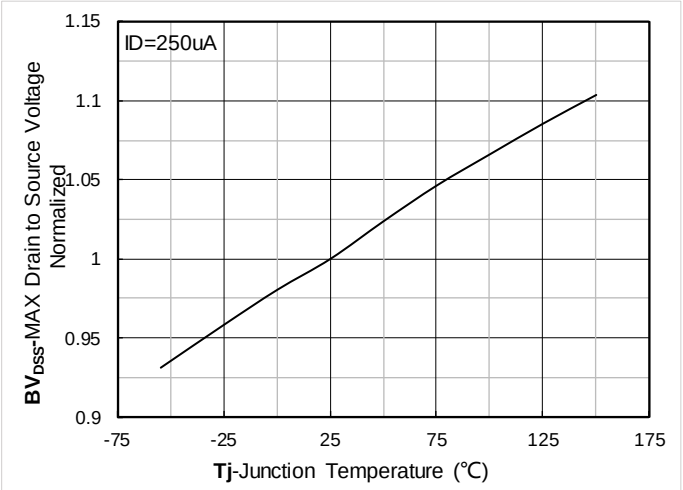


Figure 9. Normalized breakdown voltage

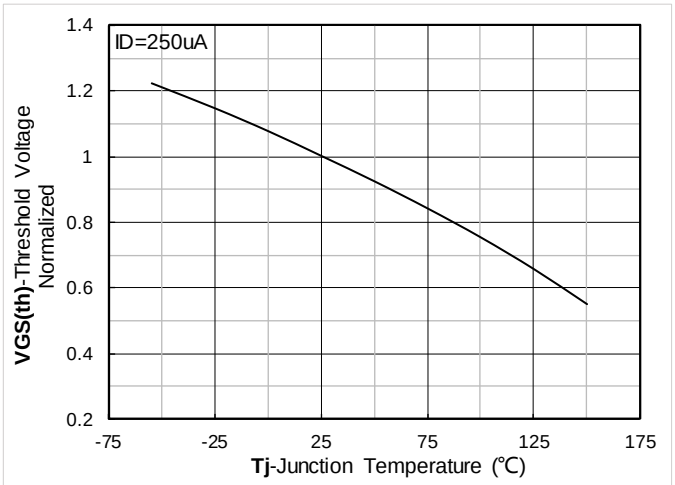


Figure 10. Normalized Threshold voltage

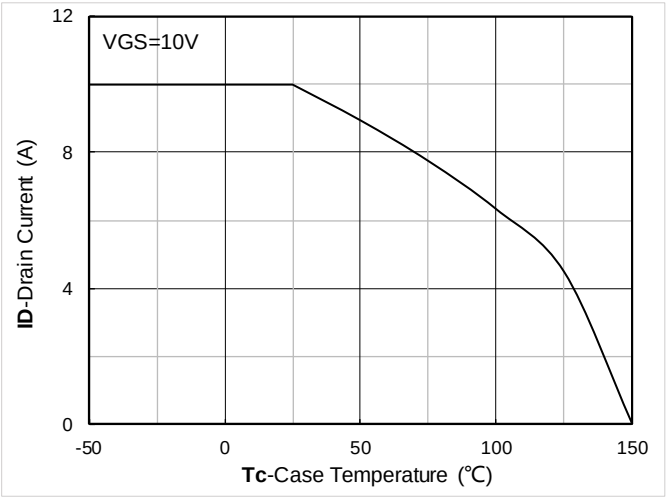


Figure 11. Current dissipation

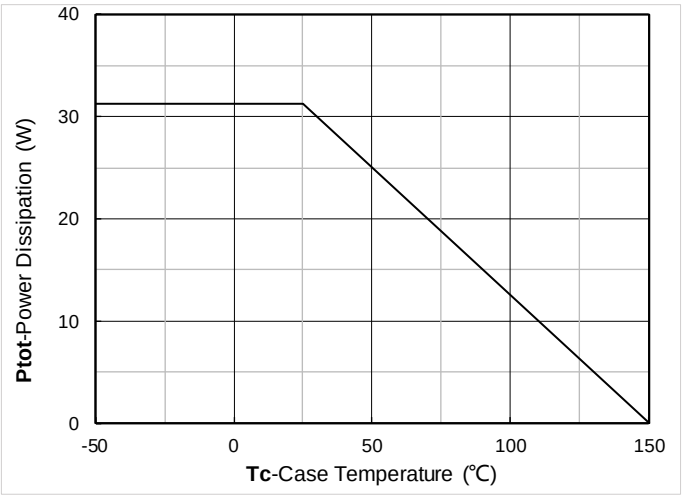


Figure 12. Power dissipation

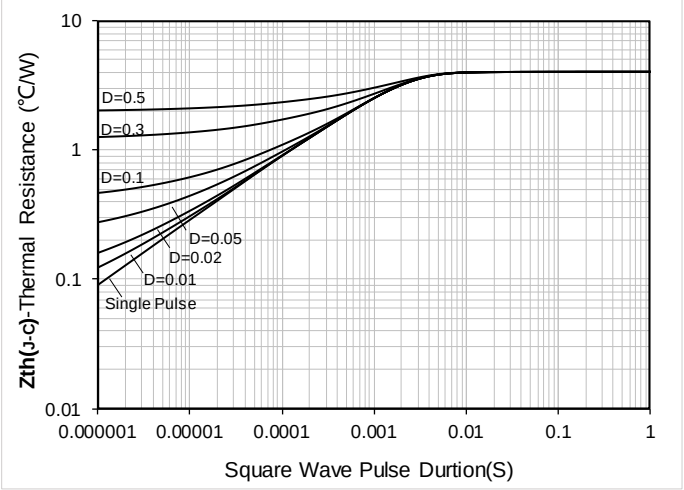


Figure 13. Maximum Transient Thermal Impedance

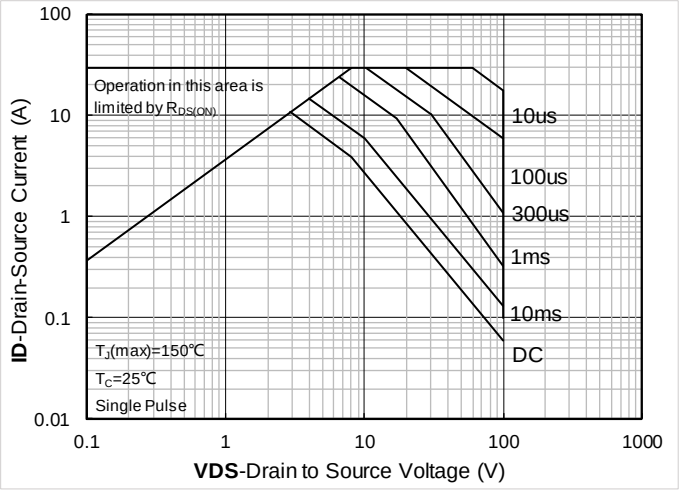


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

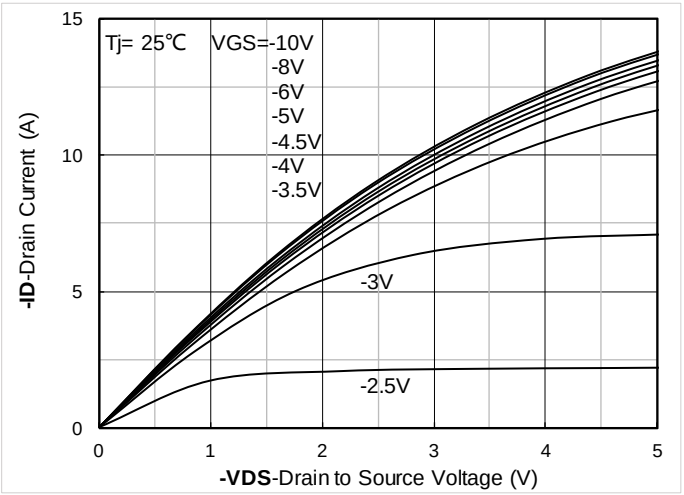


Figure 1. Output Characteristics; typical values

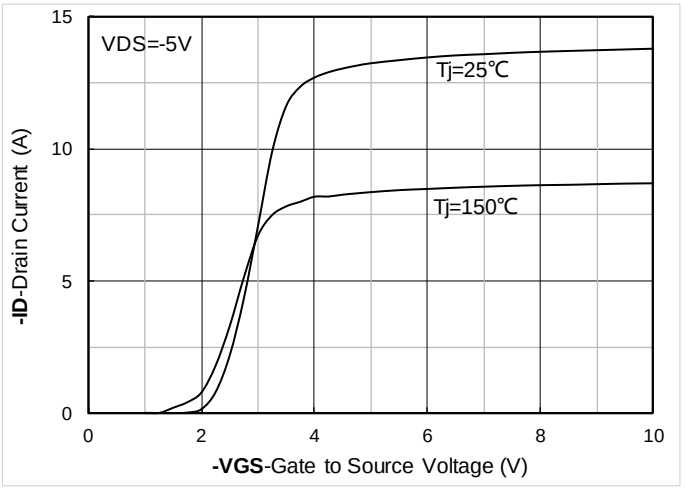


Figure 2. Transfer Characteristics; typical values

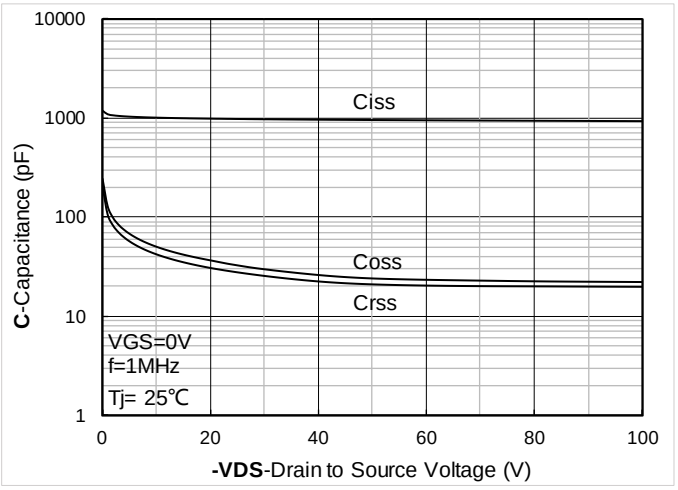


Figure 3. Capacitance Characteristics; typical values

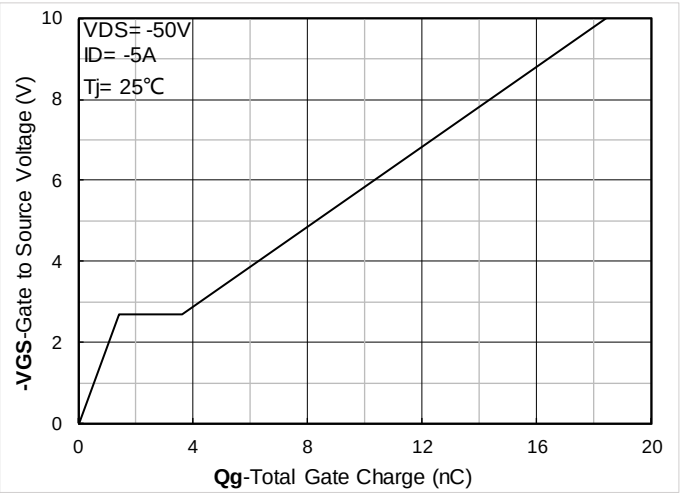


Figure 4. Gate Charge; typical values

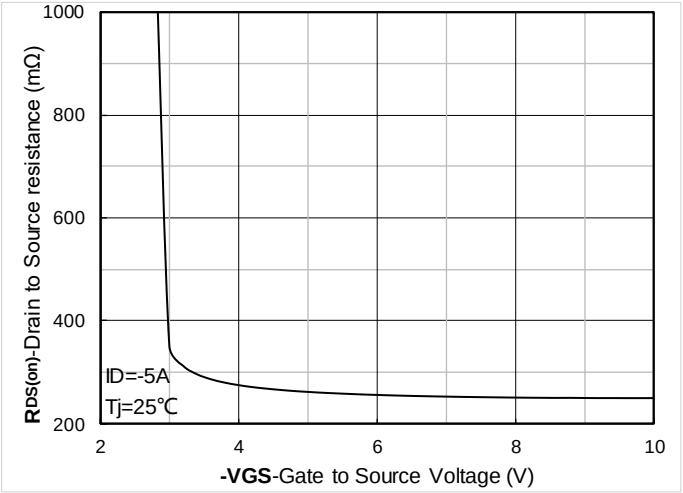


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

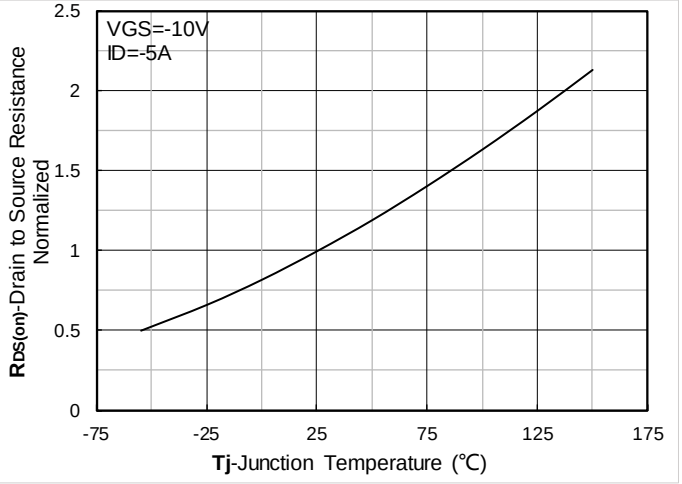


Figure 6. Normalized On-Resistance

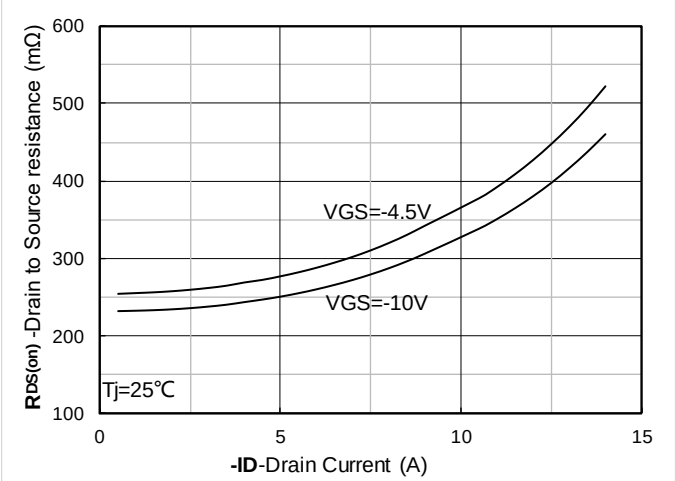


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

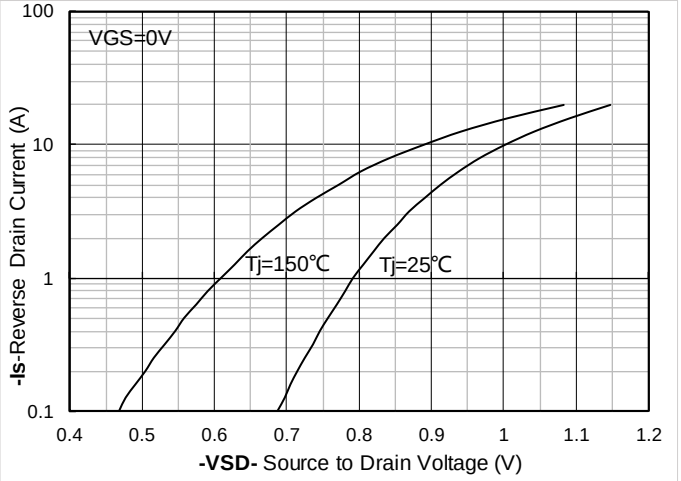


Figure 8. Forward characteristics of reverse diode; typical values

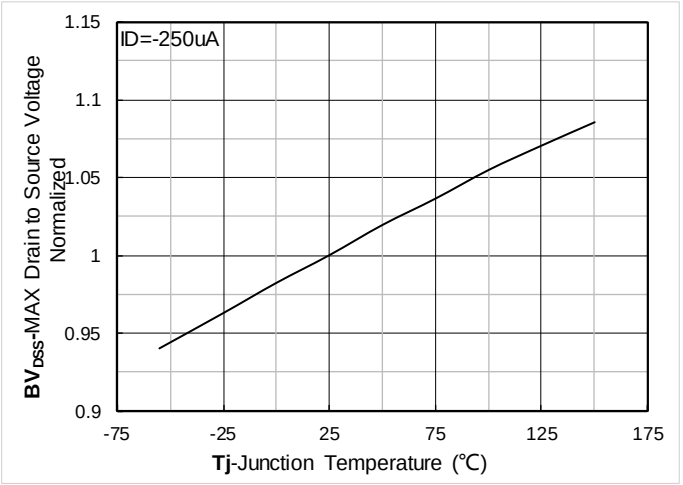


Figure 9. Normalized breakdown voltage

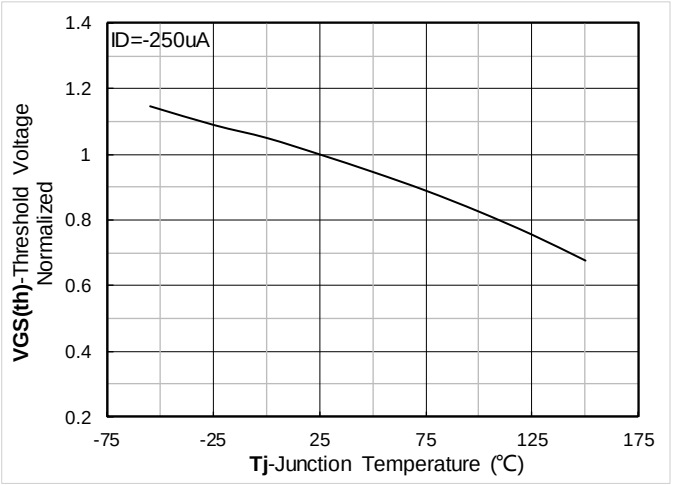


Figure 10. Normalized Threshold voltage

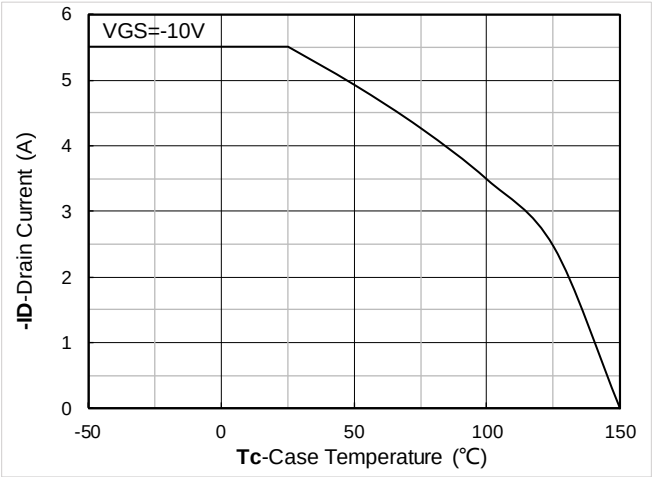


Figure 11. Current dissipation

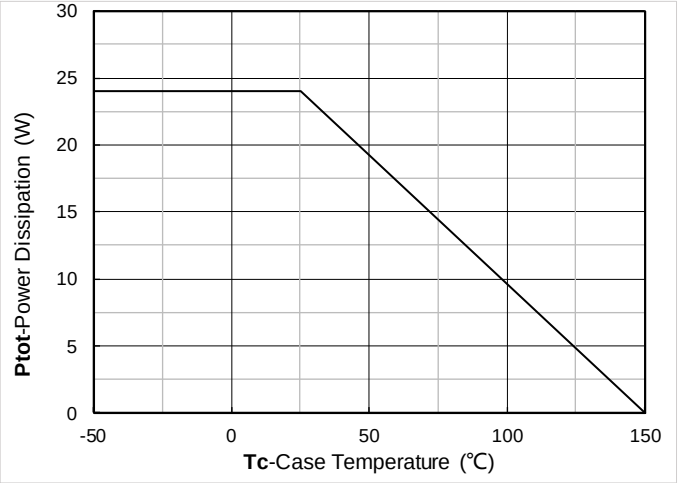


Figure 12. Power dissipation

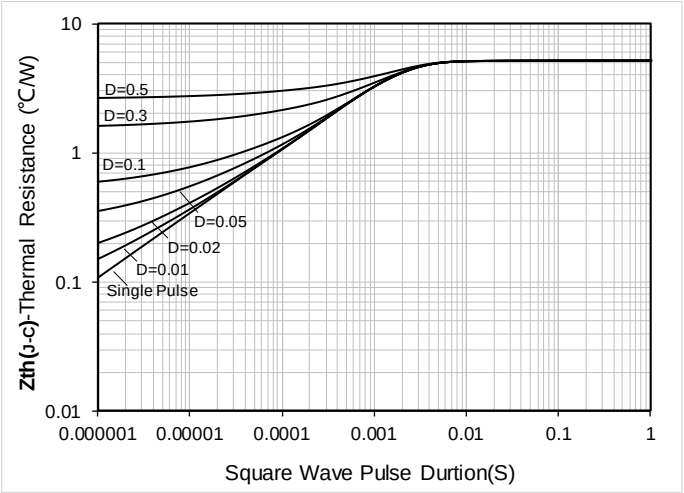


Figure 13. Maximum Transient Thermal Impedance

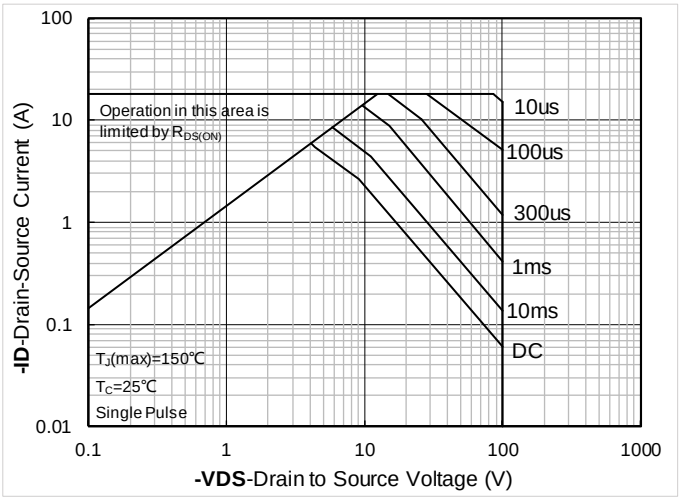
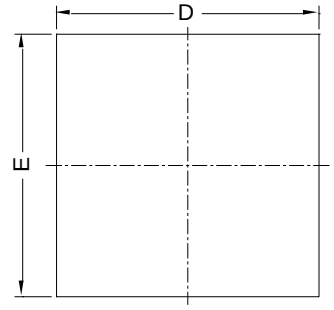
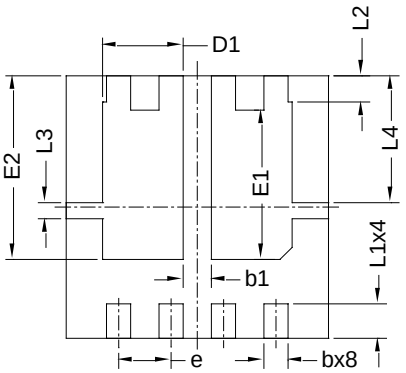


Figure 14. Safe Operation Area

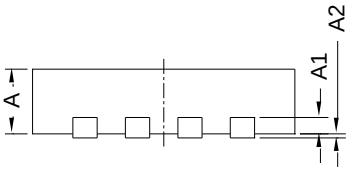
■ DFN3333-8L-B-0.8MM Package information



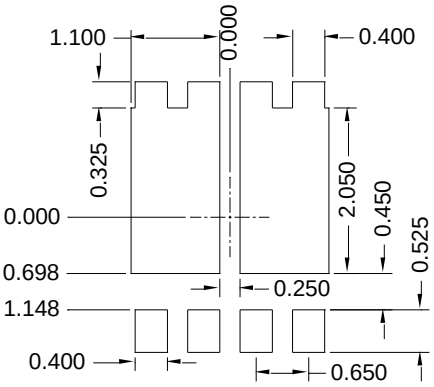
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图

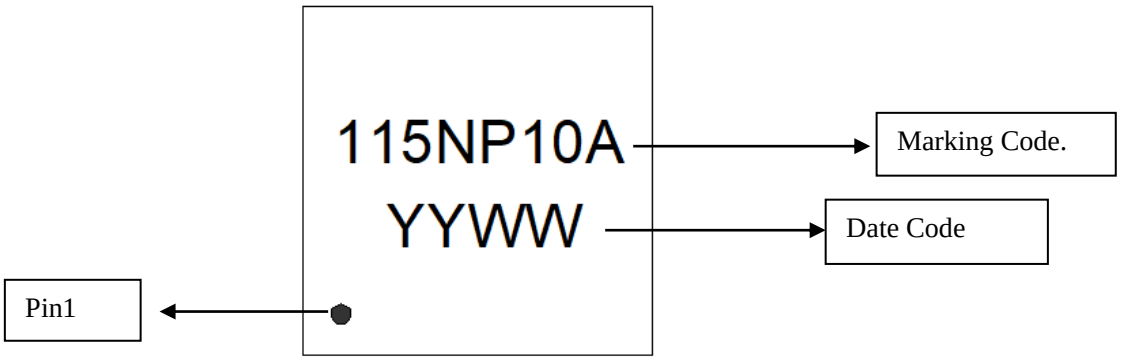


Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
E2	2.175	2.275	2.375
L1	0.325	0.425	0.525
L2		0.325 BSC	
L3		0.200 BSC	
L4		1.570 BSC	
b	0.20	0.30	0.40
e		0.65 BSC	
b1		0.35 REF	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

■**Marking**



Note：
1. All marking is at middle of the product body
2. All marking is in laser printing
3. 115NP10A is marking code, YYWW is date code, “YY” is year, “WW” is week
4. Body color: Black

Disclaimer

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The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of with would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), Yangjie or anyone on its behalf, assumes no responsibility or liability for any damages resulting from such improper use of sale.

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